Advanced Design of Broadband Distributed Amplifier using a SiGe BiCMOS Technology

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Abstract – **In this paper, we present the design of an integrated distributed amplifier for optical communication applications using SiGe BiCMOS technology. The design of some of the passive devices of the circuit has been achieved from full-wave electromagnetic simulation and novel equivalent circuit. We considered discontinuity effects to reduce parasitics at high frequency. The designed SiGe BiCMOS exhibit an available power again of 7 dB from 0.5 GHz to 22 GHz. The accurate electromagnetic consideration can be applied to System-On-Chip application in order to reduce parasitics.**

I. INTRODUCTION

Recent advances in integration technology and device performance paved the way for higher level of System integration On Chip (SOC). Theses requirements are critical for some specific application such as high speed and high frequency digital optic communication to reduce the cost and size of communication system. The distributed amplifier is recognized as one of the most popular broadband amplifier configurations. For the past several years, GaAs or InP based distributed amplifiers have dominated the broadband amplifier market. However, GaAs-based integrated circuits are relatively expensive. Moreover, since future system-on-chip solutions will comprise tens of millions of digital gates as well as analog/digital and RF interfaces, it is essential that RF/microwave circuits be implemented in low-cost silicon technology. However, silicon suffers from large parasitic elements both in active and passive devices, and therefore new design techniques are needed at such high frequencies. Main obstacles in the design of a silicon-based distributed amplifier are the low quality factor on-chip spiral inductor and transmission line. A single ended CMOS RF distributed amplifier using bond-wire inductors was presented with a gain of 5 dB over 300 kHz to 3 GHz [1]. It utilized bond-wire as high quality inductors to reduce parasitic effects. In another work, CMOS distributed amplifier with on-chip spiral inductor was created in 0.6 μm three layer-metal digital CMOS process [2]. 0.18 μm CMOS distributed amplifier with Coplanar Strip (CPS) was designed with the unity gain-bandwidth product of 23 GHz [3]. However, conventional circuit design methodology is not suitable for high-speed / high-frequency distributed amplifier. High frequency distributed amplifier needs enough electromagnetic consideration for high quality factor on-chip spiral inductor.

In this paper, we present the design and the characterization of a distributed amplifier for optical communication using SiGe BiCMOS technology. Proposed distributed amplifier is designed based on electromagnetic simulations and novel equivalent circuit to accurately design the op-chip spiral inductor. In addition, we considered discontinuity effects to reduce parasitics at high frequency. The designed SiGe BiCMOS distributed amplifier shows the good small-signal gain performance up to high frequency. Design and analysis of the distributed amplifier will be presented.

II. HIGH-Q ON-CHIP SPIRAL INDUCTOR

Fig. 1 shows the standard model components and losses of an on-chip inductor. L_s presents the series inductance of the inductor, R_s the series DC resistance, C_{ox} oxide capacitance, C_{si} the substrate capacitances, R_{si} is the substrate resistances, C_p the fringing capacitance between the metal traces. The topology of this model is similar to that of typical on-chip inductor model. However, there are two additional components to represent the eddy current loss in the Si substrate. L_{eddy} is the inductance of eddy current that reduces the effective inductance value and R_{eddy} is the ac losses due to inductance magnetic coupling to the substrate. M_{12} presents the mutual inductance between the inductor and eddy-current substrate inductance. Electric energy is coupled to the substrate through displacement current. The substrate losses arises from the displacement current flowing through the oxide and conduction current through the substrate to nearby

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grounds, either at the surface of the substrate or at the back plane of the substrate. Induced current flows in the substrate due to the time-varying electric field from the inductor, which induces substrate current [4]. The resistance of metal lines causes the inductor to have a high series resistance limiting its performance at low frequencies, while the capacitive coupling to the lossy silicon substrate is responsible for the degradation of the Q factor at higher frequencies.

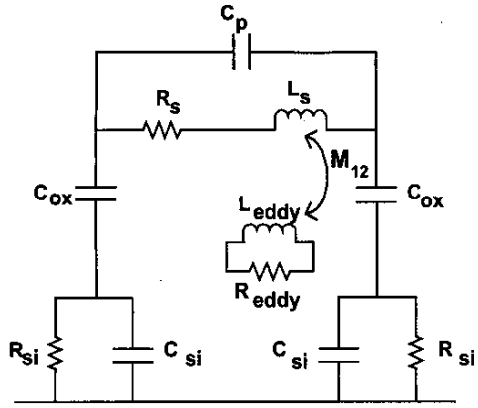

Fig. 1. Equivalent circuit of silicon based inductor with eddy current effects.

The s-parameters for the inductor equivalent circuit is simulated on circuit simulation ADS. We used fitted model parameter from [5] to compare the different loss mechanism associated with the inductor structure. Eddy current and dielectric loss effects in lossy Si substrate are shown separately in Fig. 2.

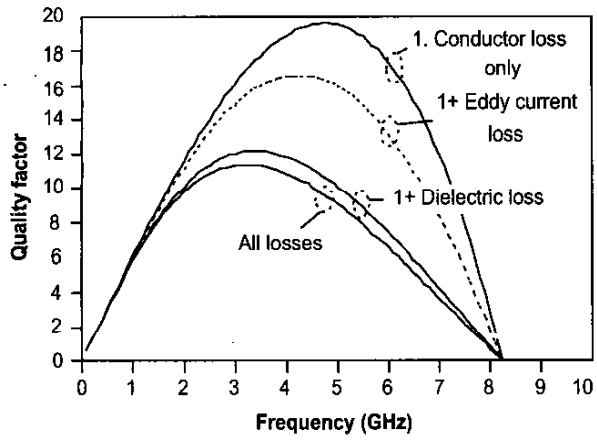

Fig. 2 Quality-factor for inductance on lossy Si substrate with different type of loss mechanism.

The metal conductor loss is first simulated without the eddy current and substrate losses by removing R_{si}, R_{eddy} and L_{eddy}. Next, The conductor plus the eddy current loss are simulated by neglecting R_{si}. The conductor plus the lossy Si substrate losses are simulated by removing R_{eddy} and L_{eddy} components. Finally, all the losses associated with the inductor structure on lossy Si substrate are calculated. The substrate losses arise from the displacement current flowing through the oxide and conduction current through the substrate to nearby grounds, either at the surface of the substrate or at the back plane of the substrate. Induced current flows in the substrate due to the time-varying electric field from the inductor, which induces substrate current [4]. The resistance of metal lines causes the inductor to have a high series resistance limiting its performance at low frequencies, while the capacitive coupling to the lossy silicon substrate is responsible for the degradation of the Q factor at higher frequencies. Magnetic coupling is one of the biggest effects to degrade Q-factor of on-chip inductor. Eddy currents form in conductive material that is orthogonal to the magnetic field. On-chip inductance is fabricated and measured. The inductor metal line width equals to 10.7 μm with 3 μm thickness and 2.1 μm spacing between the metal lines. The measured value for the inductance is 2.4 nH with 4.5 turns. The Si substrate height equals to 271 μm. The inductor metals are insulated from the lossy silicon substrate by SiO_2 with 4 um thickness. The two-port s-parameters for the spiral inductors are measured using HP 8510C vector network analyzer. SOLT calibration has been performed from 0.1 GHz to 20 GHz, using an impedance standard substrate as well as calibrating standard structures on the Si substrate. The inductance s-parameters are then de-embedded from the measured s-parameters using a combination of cascade and y-parameters de-embedding. The same inductors were simulated by a full-wave electromagnetic simulator to compare measurement and simulation results.

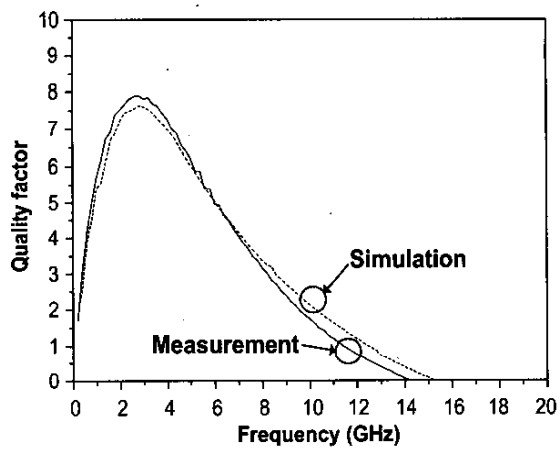

Fig. 3. Measured versus Simulated Quality factor.

Fig 3 shows the quality factor obtained from the measured and simulated input admittance. The quality factor is defined as Q = -Imag (Y_{11}) / Real (Y_{11}). It is clear that good correlation exists between the measured and the electromagnetic simulated results.

III. DESIGN DISTRIBUTED AMPLIFIER WITH HIGH FREQUENCY SIMULATION

The process used for the design was a 0.18 μm SiGe BiCMOS process with six-layer metal interconnects [6]. The final tow layers of metal are formed by thick copper which can be used to realize low loss inductors and interconnects and probed high current density carrying capability for ease of routing both signal and supply lines. A basic four-stage distributed amplifier would take the form shown in Fig. 4.

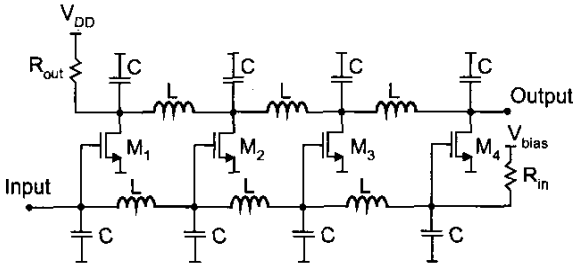

Fig. 4 Schematic of the basic distributed amplifier.

The gate and drain impedances of the FET's are absorbed into lossy artificial transmission lines formed by using lumped inductor or transmission line. The artificial transmission lines consist of the inductance of transmission line and the capacitances of transistors. In this configuration, RF signal will be coupled by the transconductance of the active device and finally RF signal will be terminated by the matched output load port. If the phase velocities on the gate and drain lines are identical, then the signals on the drain line add in the forward direction are absorbed by terminations matched to loaded characteristic impedance of the gate line impedance. The MOSFET gate resistance R_g was minimized to reduce gate artificial transmission line loss in the distributed amplifier. The input capacitance was also minimized to increase input transmission line cutoff frequency. Four MOSFET unit cells were used as active elements in the distributed amplifier. Each unit cell consisted of 40 fingers with dimensions of 4 μm x 0.36 μm per finger for a total gate width of 160 μm. The *n*-MOSFETs at the bias point had a transconductance of 40.52 mS and input capacitance of 53.9 fF per micron gate width. In addition, R_g of 1.437 Ω and Rs of 2.9 Ω were used in the simulation. Assuming phase synchronization and using image-impedance-matched terminations, the voltage gain can be derived as [2]

$$\frac{V_{out}}{V_{in}} = \frac{N \cdot g_m}{2\sqrt{1-\omega^2/\omega_c^2}}\sqrt{\frac{L}{C}}e^{-N\theta} \quad (1)$$

However, designed distributed amplifier has degraded performance at high frequency. The parasitic effects at high frequency degrade the performance in two ways. First is the inherent loss and capacitive parasitic effects of the on-chip spiral inductors. The large capacitive parasitic of the inductors act to disrupt phase synchronization between the gate and drain lines. In addition, discontinuity effects at high frequency increase discontinuity loss and phase variation. To solve these problems, we use 3-D high frequency electromagnetic simulation and novel inductor equivalent circuit, which includes eddy current effects. Discontinuity and interconnection effects are considered and optimized using Agilent ADS software. These effects are one of main problems degrading the performance of distributed amplifier at high frequency.

IV. RESULTS AND DISCUSSIONS

The distributed amplifier is designed in 0.18 μm SiGe BiCMOS technology using only CMOS transistors. The top metal layer is 3 μm thick and 7.25 μm above substrate. On-chip spiral inductor parameters from full-wave electromagnetic simulations and high frequency discontinuity effects are used to simulate accurate artificial transmission line. Fig. 5 shows the S-parameter response. The gain is 7 dB with ± 0.7dB flatness from 0.5 GHz to 22 GHz. The input match has a worst-case value of – 8 dB at 3 GHz, and is generally –10 dB or better over most of the bandwidth. The increase in gain in low frequency was due to the higher impedance of the blocking capacitance at low frequency. All simulations were taken under identical DC bias conditions, 3 V on the drain line and 2 V on the gate line; at this bias point the distributed amplifier consumed 43 mA for a total power dissipation of 132 mW. The VSWR is less than 2.12:1 throughout the operating frequency range. The phase response of this circuit is shown in Fig. 6. Result shows linear variation up to cutoff frequency. The noise figure was simulated up to 20 GHz. The results are shown in Fig. 7. Averaging the results over the bandwidth yields a noise figure of 8 dB. Fig 8 shows the layout of the complete distributed amplifier. The distributed amplifier occupies an area of 1.8 mm x 1 mm, which include the pad frame. Due to very high frequency operation, special attention should be paid to the layout [7]. Thus, enough design accuracy can be achieved by

adding accurate high-Q inductor model and optimizing parasitic effects come from discontinuity and interconnection.

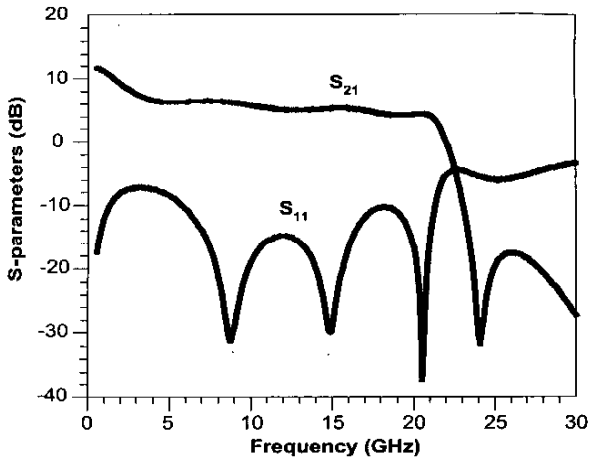

Fig. 5 S-parameters of the distributed amplifier.

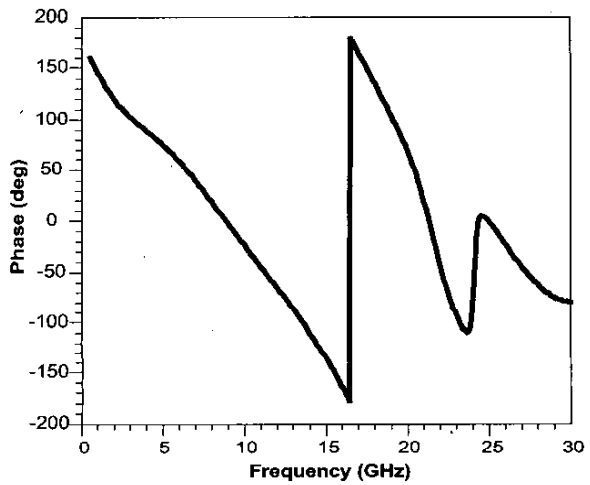

Fig. 6 Phase response of the distributed amplifier.

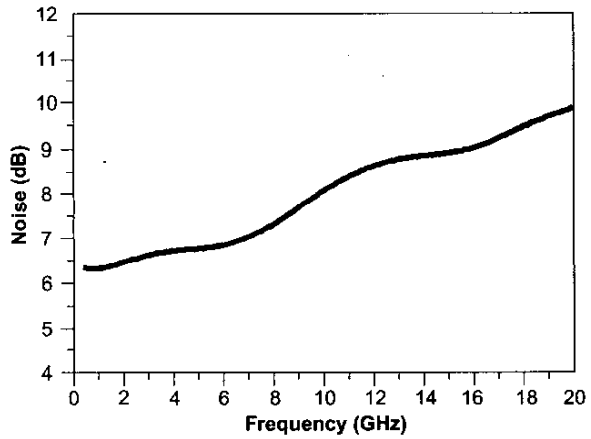

Fig. 7 Noise Figure of the distributed amplifier.

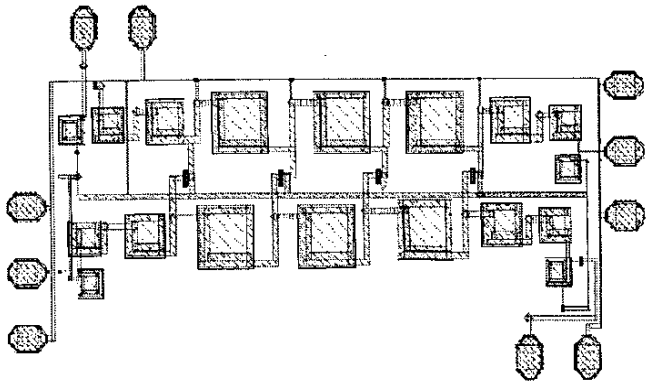

Fig. 8 Layout of the distributed amplifier.

V. CONCLUSION

This paper presents the design and the characterization of a distributed amplifier for optical communication using SiGe BiCMOS technology. First of all, we have demonstrated that electromagnetic simulations and novel equivalent circuit are very important to accurately design the op-chip spiral inductor. The second point we considered discontinuity effects to reduce parasitics at high frequency. The designed SiGe BiCMOS distributed amplifier shows the good small-signal gain performance up to high frequency. The accurate electromagnetic consideration can be applied to System-On-Chip application in order to reduce parasitic effects.

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